Sub D2

silicon are interspaced between said isolation oxides to form a shallow trench isolation (STI) structure.

Sub C2

31. The semiconductor device according to claim 30, wherein said SOI region further comprises:

an insulator layer underneath said STI structure.

32. The semiconductor device according to claim 29, wherein said amorphous silicon is crystallized using an exposed portion of silicon as a seed.

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33. The semiconductor device according to claim 30, wherein isolation oxides are formed between adjacent devices on said semiconductor device.

Sub C3

34. The semiconductor device according to claim 31, wherein said insulation oxides and said insulator layer are formed of a same material.

Sub D3

35. The semiconductor device according to claim 29, wherein

an upper surface of said isolation oxides and said crystallized silicon layer are planarized.

36. The semiconductor device according to claim 29, wherein said crystallized silicon layer has a crystal orientation and structure which follows that of an underlying substrate.

37. The semiconductor device according to claim 29, further comprising:

a memory device formed in said bulk silicon region; and

a logic device formed in said SOI region.

Sub F3

38. The semiconductor device according to claim 37, wherein said memory device comprises at least one of a dynamic random access memory (DRAM) device, a memory array, a static random access memory (SRAM) device, a flash memory device, a high voltage,

high power circuit, and an analog circuit.

39. The semiconductor device according to claim 37, wherein said logic device comprises at least one of a logic circuit, a P-FET device, an N-FET device, a low voltage, low power circuit, and a high performance digital circuit.

40. A semiconductor device comprising:

a bulk silicon region; and

a silicon-on-insulator (SOI) region comprising:

a crystallized silicon layer formed by annealing a silicon germanium layer and having isolation trenches formed therein so as to remove defective regions, and

isolation oxides formed in said isolation trenches.

41. A hybrid bulk silicon and silicon-on-insulator (SOI) substrate, comprising:

a crystallized silicon layer formed by annealing amorphous silicon and having isolation trenches formed therein so as to remove defective regions; and

isolation oxides formed in said isolation trenches.

42. The hybrid substrate according to claim 41, further comprising:

a bulk silicon region; and

an SOI region,

wherein said crystallized silicon layer and said isolation oxides are formed in said SOI region.

43. The hybrid substrate according to claim 42, wherein a logic device is formed in said silicon-on-insulator (SOI) region.

44. The substrate according to claim 42, wherein a memory device is formed in said bulk silicon region.